MEMORY RE-IMPLEMENTATION FOR FIELD PROGRAMMABLE GATE ARRAYS

Abstract of Disclosure

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Memory modules implemented on an FPGA device are re-implemented to improve the performance of the device, such as to reduce logic delays. One or more logic blocks of the FPGA device that realize the logic function of a memory module or portion of a memory module are desirably selected. Based on the outcome of a timing

10   analysis, the most critical signal pin of the selected logic blocks may be identified. Methods of deriving the memory module re-implementation for various types of the most critical pins are disclosed. Procedures are described for integrating physical timing analysis, memory transformation, placement, and routing, as well as for the selection of logic blocks for re-implementation.

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